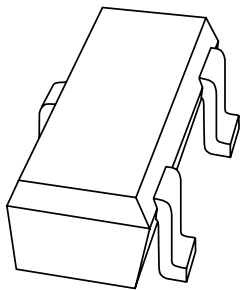


DATA SHEET



PDTA143XK

PNP resistor-equipped transistor;
R1 = 4.7 k Ω , R2 = 10 k Ω

Product specification

2002 Jan 15

PNP resistor-equipped transistor;
R1 = 4.7 kΩ, R2 = 10 kΩ

PDTA143XK

FEATURES

- Built-in bias resistors
- 250 mW total power dissipation
- Package size 2.9 × 1.5 × 1.15 mm
- Simplification of circuit design
- Reduces number of components and required PCB area.

APPLICATIONS

- General purpose switching and amplification
- Inverter and interface circuits
- Circuit driver.

DESCRIPTION

PNP resistor equipped transistor in a SOT346 (SC-59) plastic package.

MARKING

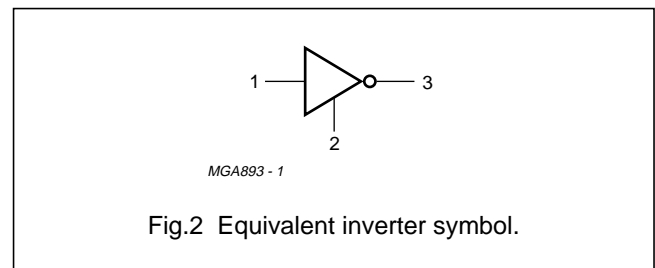
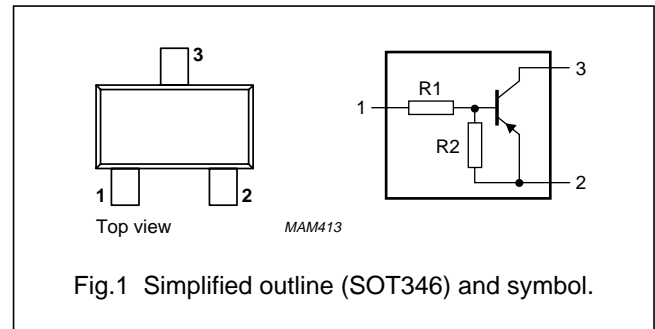
TYPE NUMBER	MARKING CODE
PDTA143XK	25

QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V _{CEO}	collector-emitter voltage	-50	V
I _O	output current (DC)	-100	mA
R1	bias resistor	4.7	kΩ
R2	bias resistor	10	kΩ

PINNING

PIN	DESCRIPTION
1	base/input
2	emitter/ground (+)
3	collector/output



PNP resistor-equipped transistor;
 $R1 = 4.7 \text{ k}\Omega$, $R2 = 10 \text{ k}\Omega$

PDTA143XK

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	–50	V
V_{CEO}	collector-emitter voltage	open base	–	–50	V
V_{EBO}	emitter-base voltage	open collector	–	–10	V
V_i	input voltage				
	positive		–	+7	V
	negative		–	–20	V
I_o	output current (DC)		–	–100	mA
I_{CM}	peak collector current		–	–100	mA
P_{tot}	total power dissipation	$T_{amb} \leq 25 \text{ }^\circ\text{C}$; note 1	–	250	mW
T_{stg}	storage temperature		–65	+150	$^\circ\text{C}$
T_j	junction temperature		–	150	$^\circ\text{C}$
T_{amb}	operating ambient temperature		–65	+150	$^\circ\text{C}$

Note

- For mounting conditions, see “*Thermal considerations and footprint design for SOT346 in the SC18 Data Handbook*”.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air; note 1	500	K/W

Note

- For mounting conditions, see “*Thermal considerations and footprint design for SOT346 in the SC18 Data Handbook*”.

PNP resistor-equipped transistor;
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PDTA143XK

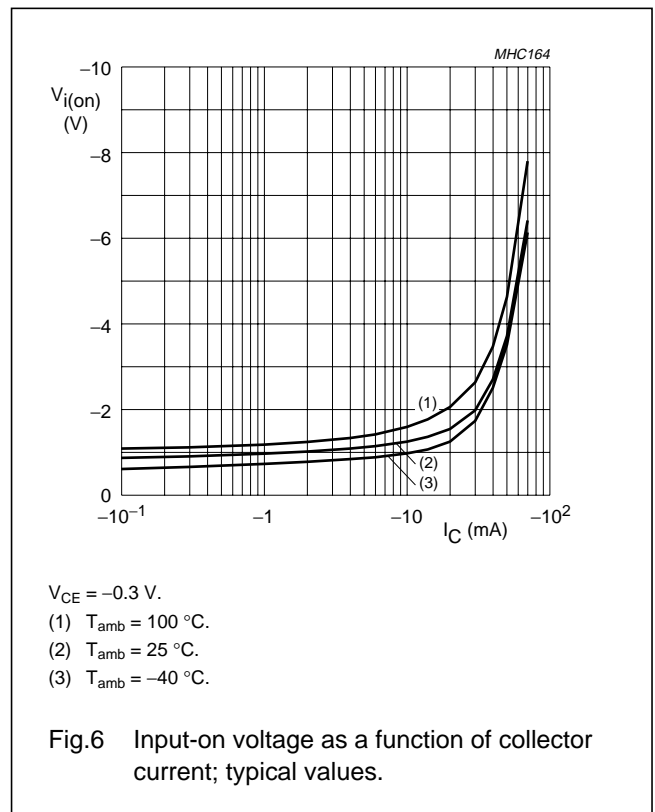
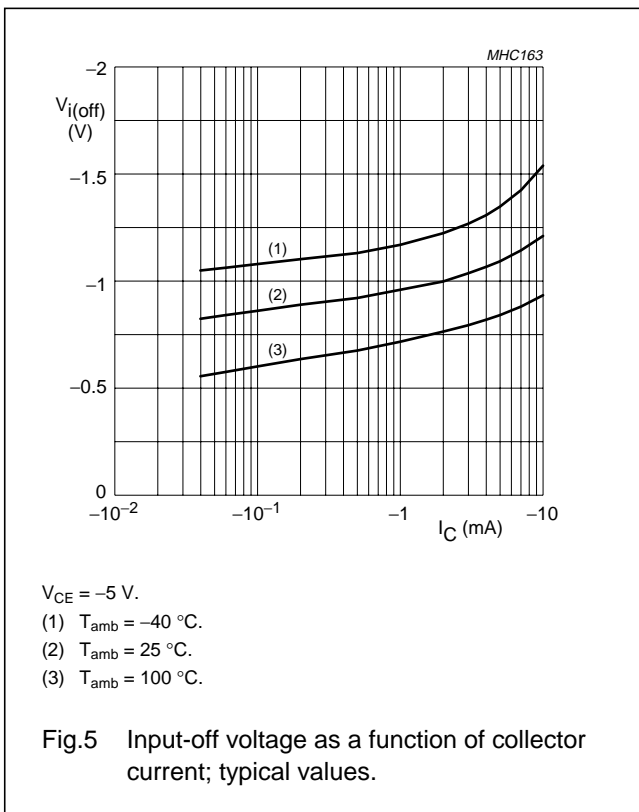
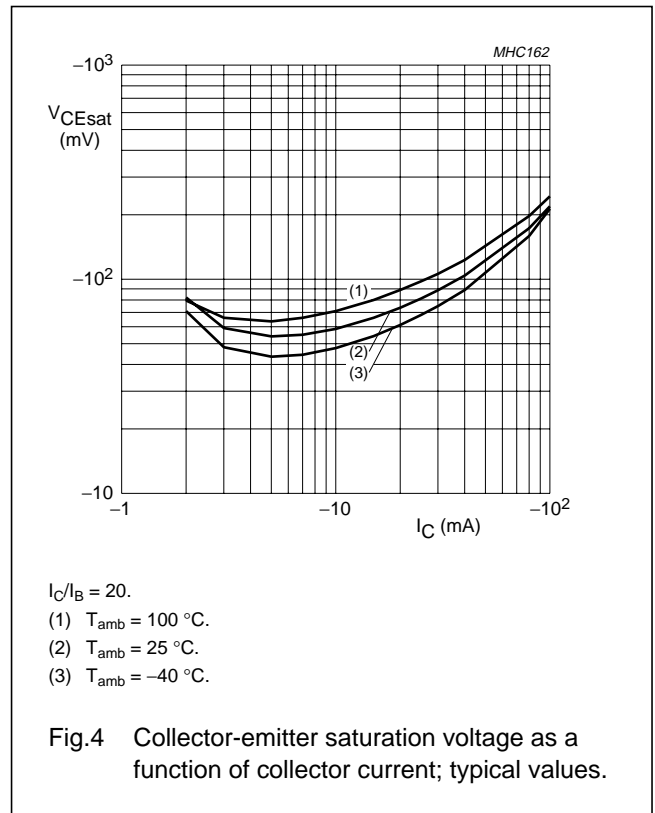
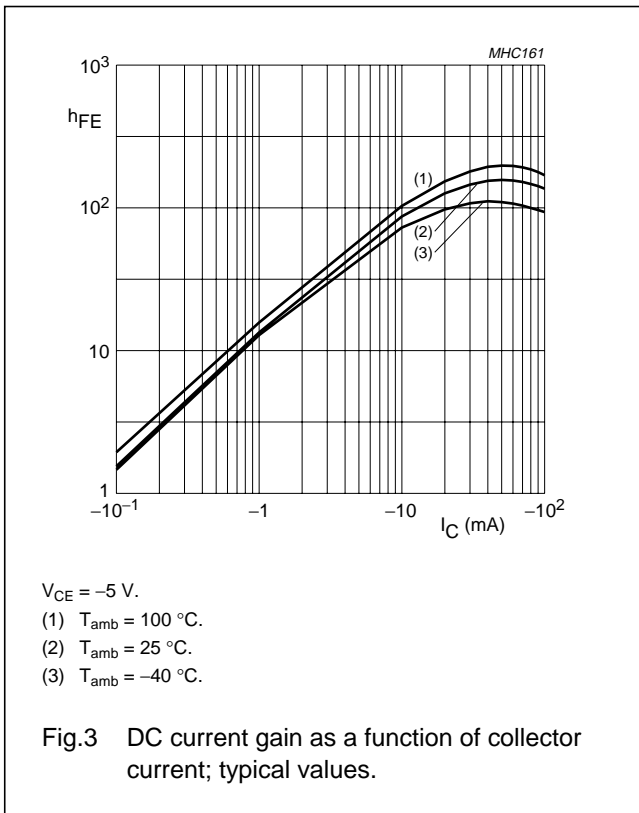
CHARACTERISTICS

$T_{\text{amb}} = 25 \text{ }^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{CBO}	collector-base cut-off current	$V_{\text{CB}} = -50 \text{ V}$; $I_{\text{E}} = 0$	–	–	–100	nA
I_{CEO}	collector-emitter cut-off current	$V_{\text{CE}} = -30 \text{ V}$; $I_{\text{B}} = 0$	–	–	–1	μA
		$V_{\text{CE}} = -30 \text{ V}$; $I_{\text{B}} = 0$; $T_{\text{j}} = 150 \text{ }^\circ\text{C}$	–	–	–50	μA
I_{EBO}	emitter-base cut-off current	$V_{\text{EB}} = -5 \text{ V}$; $I_{\text{C}} = 0$	–	–	–0.6	mA
h_{FE}	DC current gain	$V_{\text{CE}} = -5 \text{ V}$; $I_{\text{C}} = -10 \text{ mA}$	50	–	–	
V_{CEsat}	collector-emitter saturation voltage	$I_{\text{C}} = -10 \text{ mA}$; $I_{\text{B}} = -0.5 \text{ mA}$	–	–	–150	mV
$V_{\text{i(off)}}$	input off voltage	$V_{\text{CE}} = -5 \text{ V}$; $I_{\text{C}} = -100 \mu\text{A}$	–	–	–0.3	V
$V_{\text{i(on)}}$	input on voltage	$V_{\text{CE}} = -0.3 \text{ V}$; $I_{\text{C}} = -20 \text{ mA}$	–2.5	–	–	V
R1	input resistor		3.3	4.7	6.1	$\text{k}\Omega$
$\frac{R2}{R1}$	resistor ratio		1.7	2.1	2.6	
C_{c}	collector capacitance	$I_{\text{E}} = i_{\text{e}} = 0$; $V_{\text{CB}} = -10 \text{ V}$; $f = 1 \text{ MHz}$	–	–	3	pF

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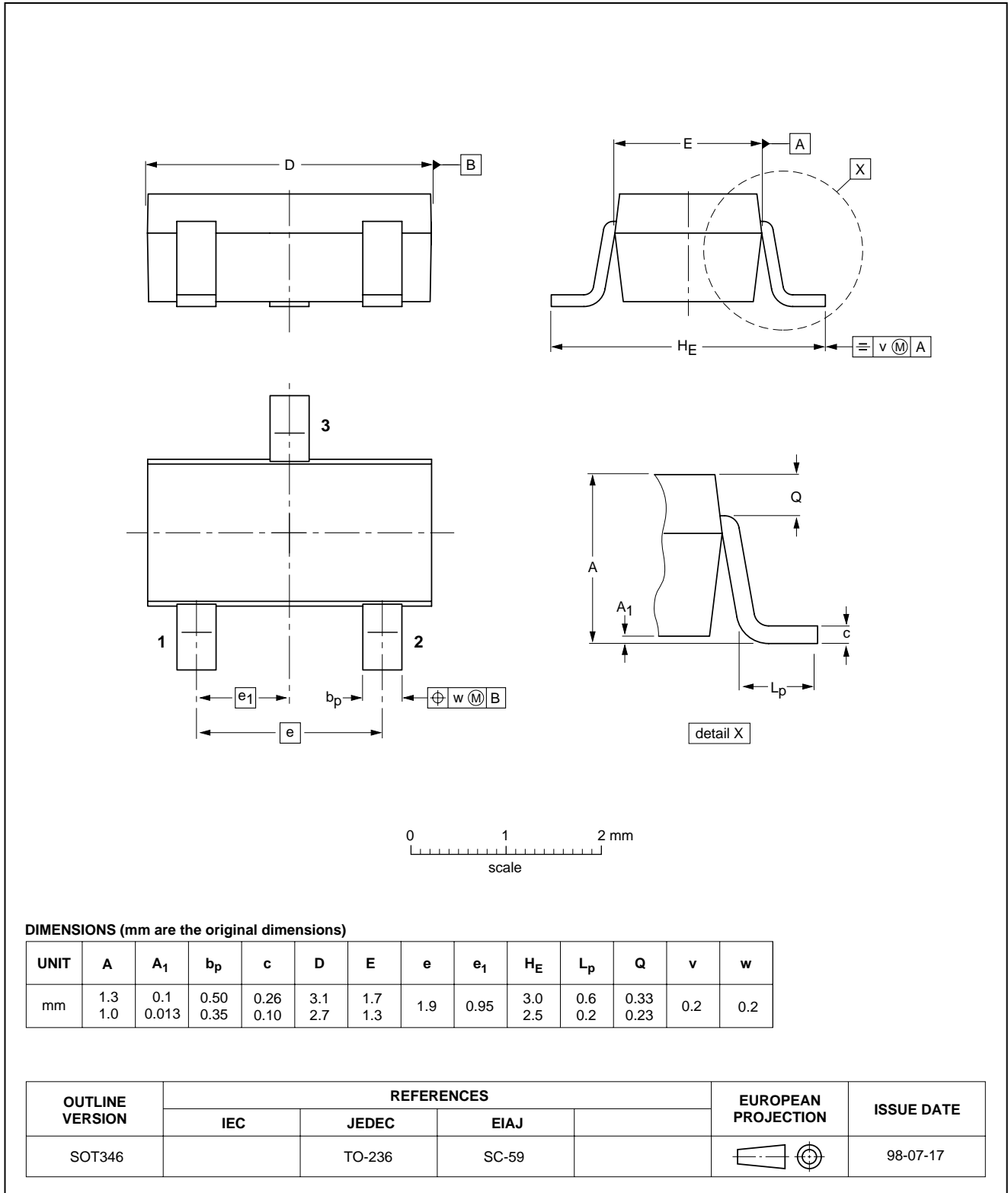
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PDTA143XK

PACKAGE OUTLINE

Plastic surface mounted package; 3 leads

SOT346



PNP resistor-equipped transistor;
R1 = 4.7 k Ω , R2 = 10 k Ω

PDTA143XK

DATA SHEET STATUS

DATA SHEET STATUS ⁽¹⁾	PRODUCT STATUS ⁽²⁾	DEFINITIONS
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